

FIG. 1A
(PRIOR ART)

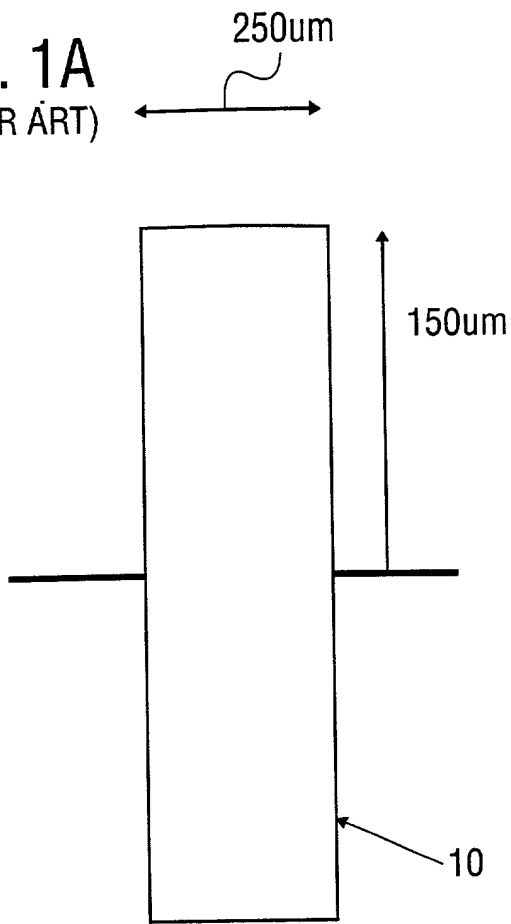


FIG. 1B
(PRIOR ART)

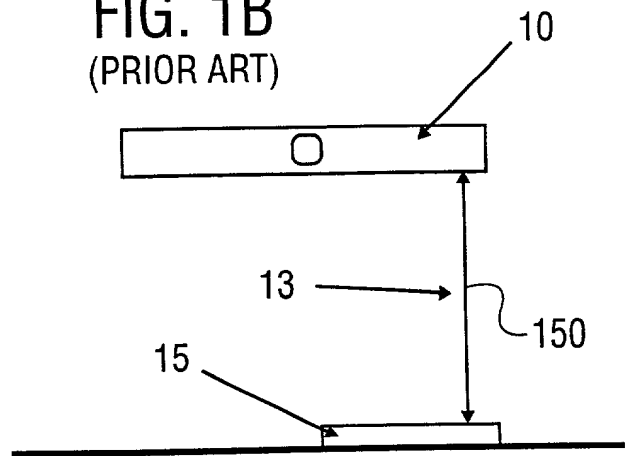
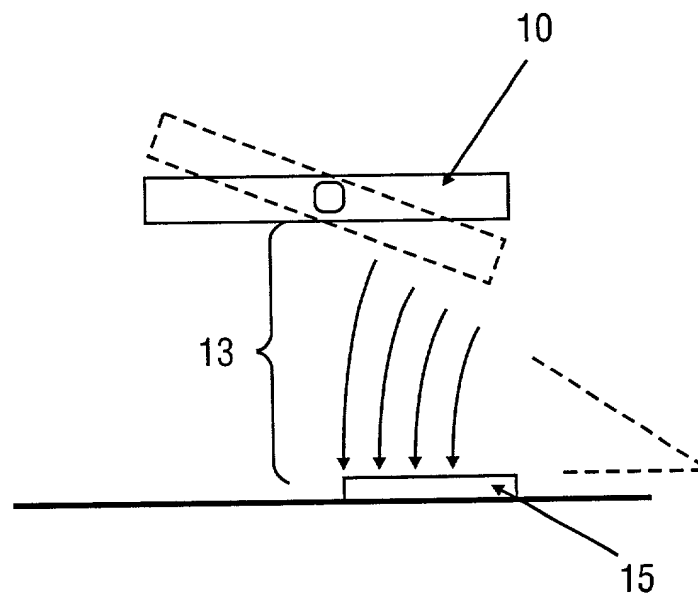
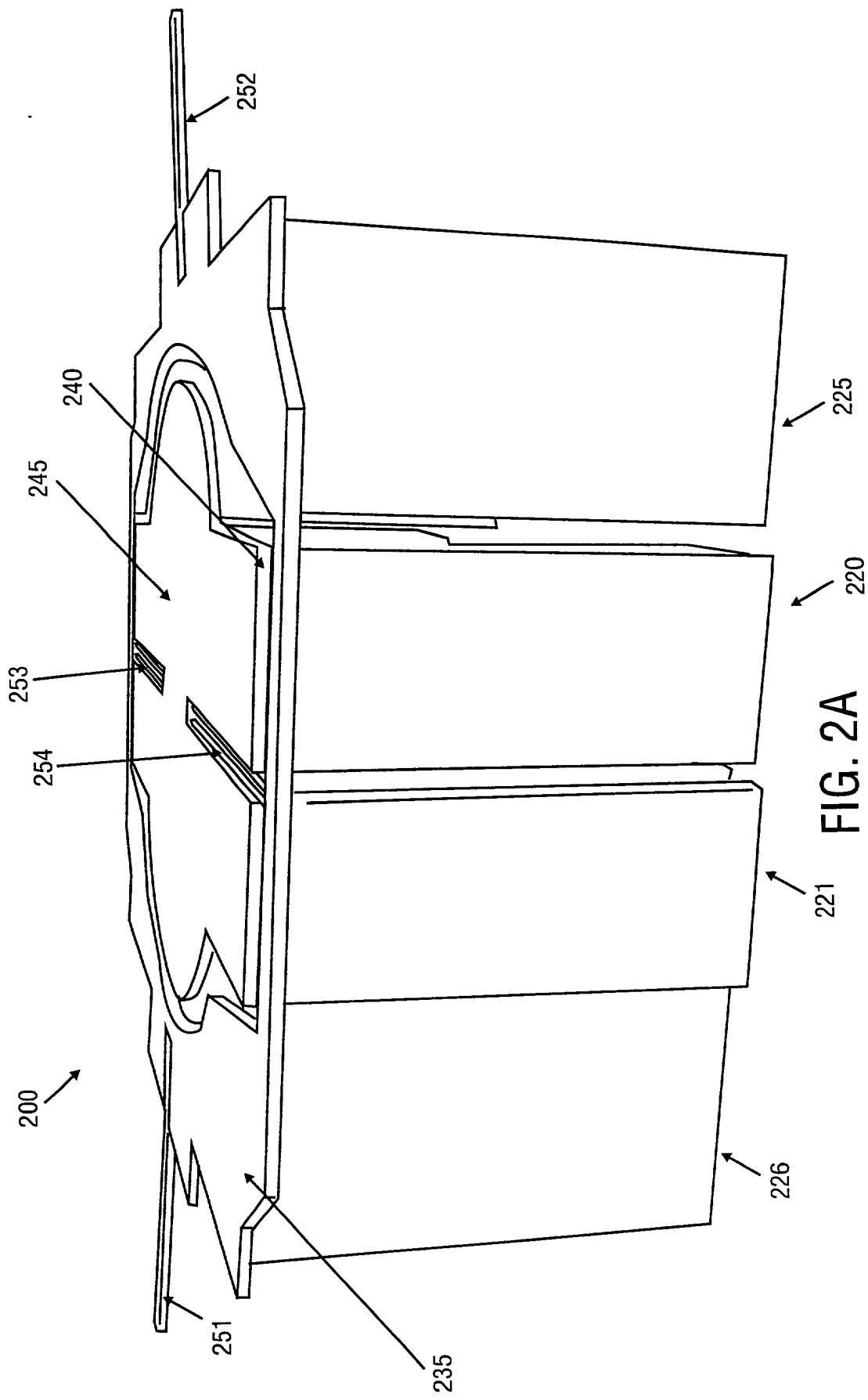


FIG. 1C
(PRIOR ART)





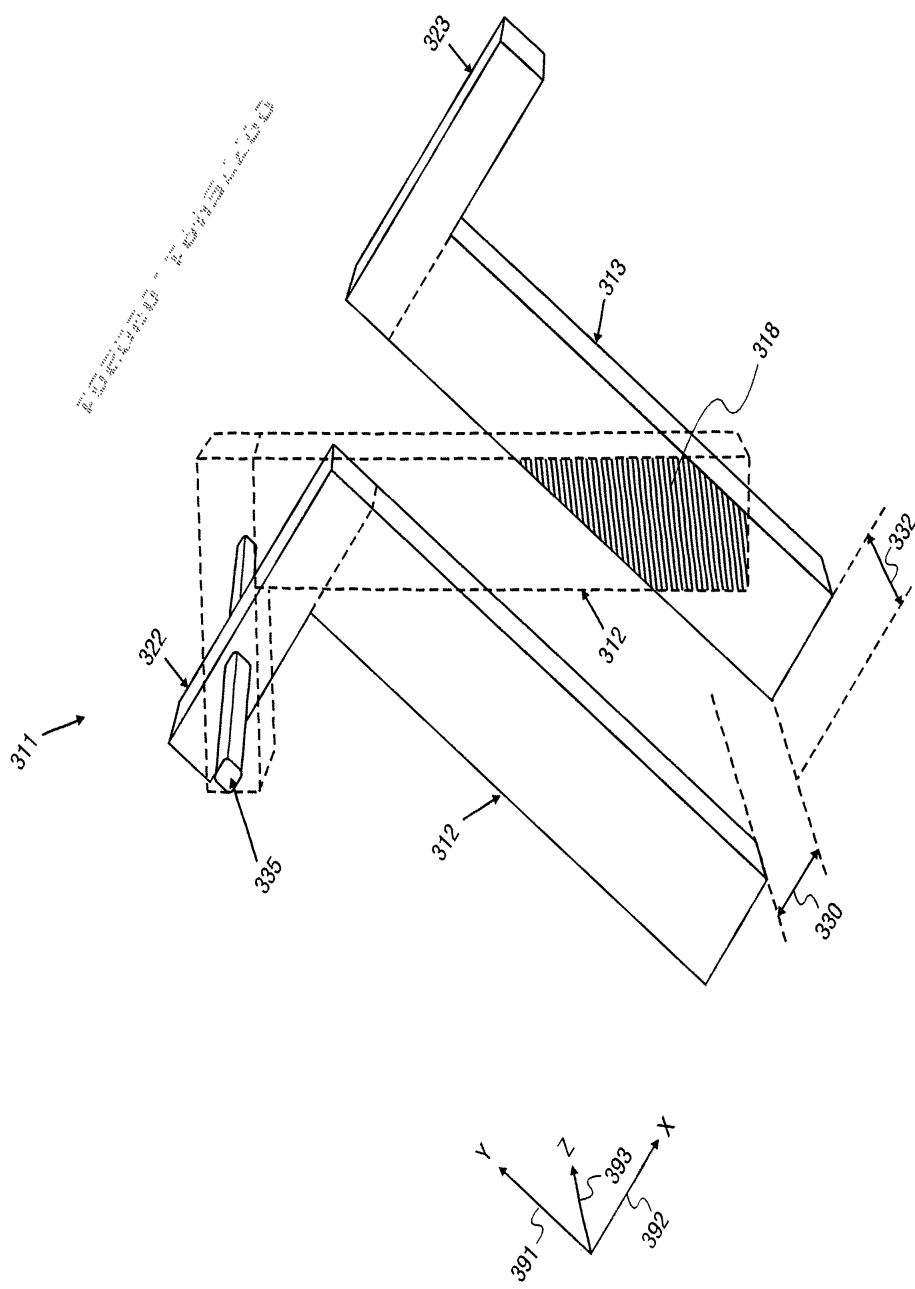


FIG. 3B

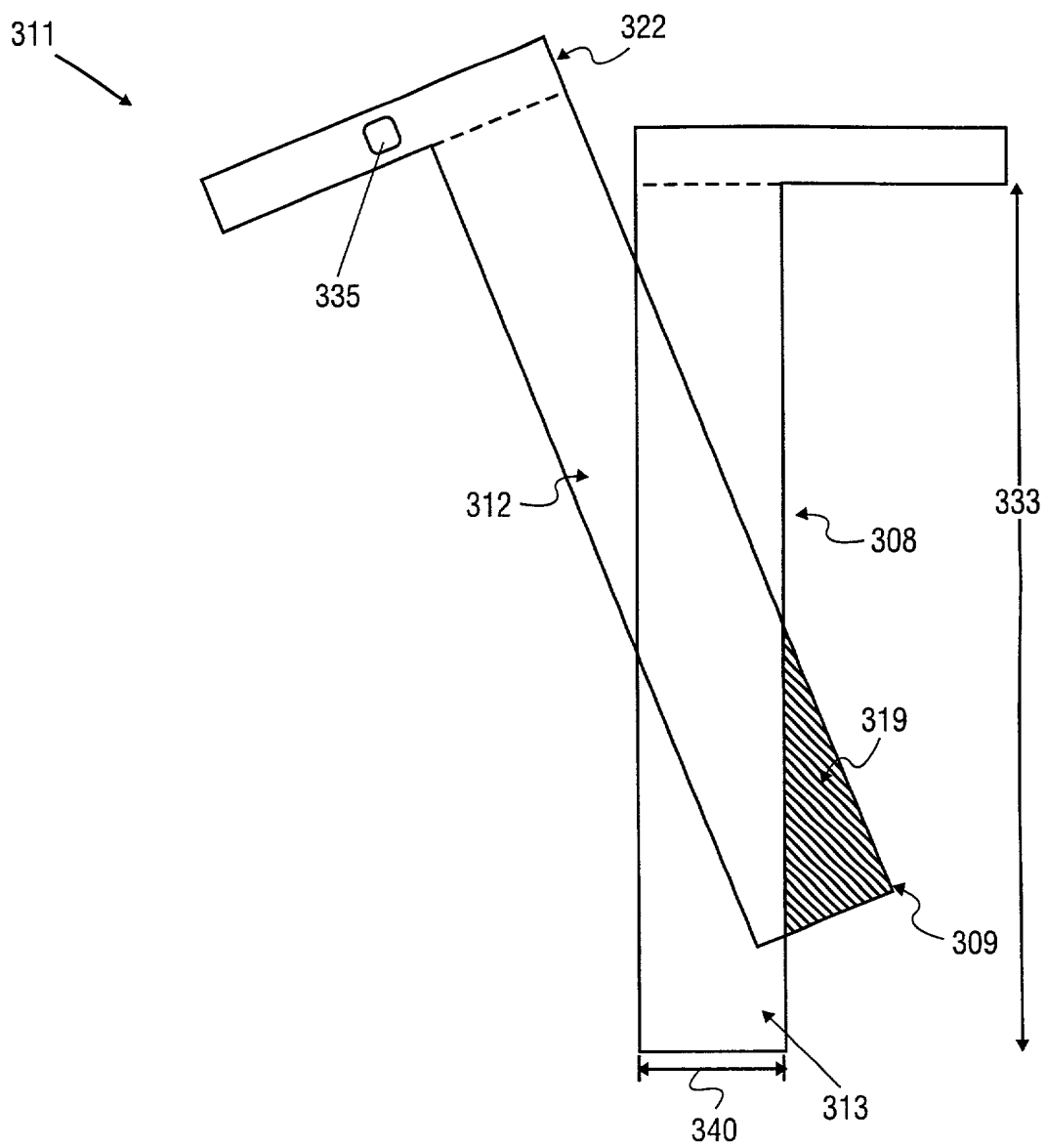


FIG. 3C

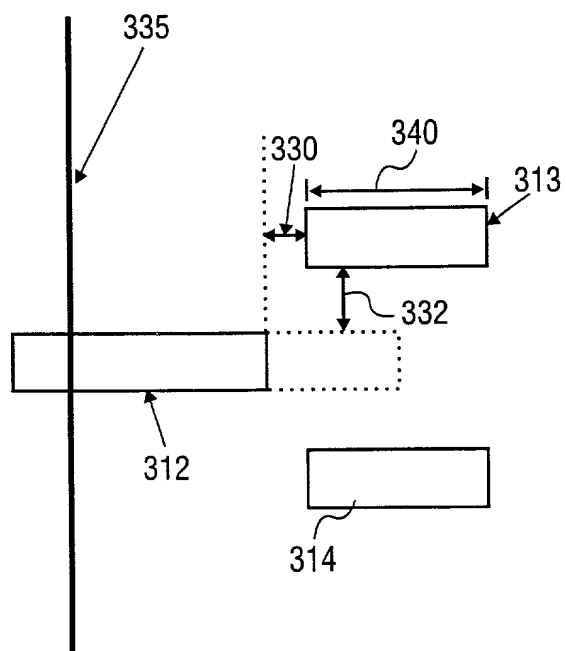


FIG. 3D

FIG. 3E is a cross-sectional view of the device 100, taken along line 3-3 of FIG. 3A. The device 100 includes a substrate 312, a first layer 313, and a second layer 329. The first layer 313 is disposed on the substrate 312, and the second layer 329 is disposed on the first layer 313. The second layer 329 includes a first portion 330 and a second portion 330. The first portion 330 is disposed on the first layer 313, and the second portion 330 is disposed on the first layer 313. The first portion 330 and the second portion 330 are separated by a gap 332. The first portion 330 and the second portion 330 are disposed on the first layer 313, and the first portion 330 and the second portion 330 are separated by a gap 332. The first portion 330 and the second portion 330 are disposed on the first layer 313, and the first portion 330 and the second portion 330 are separated by a gap 332.

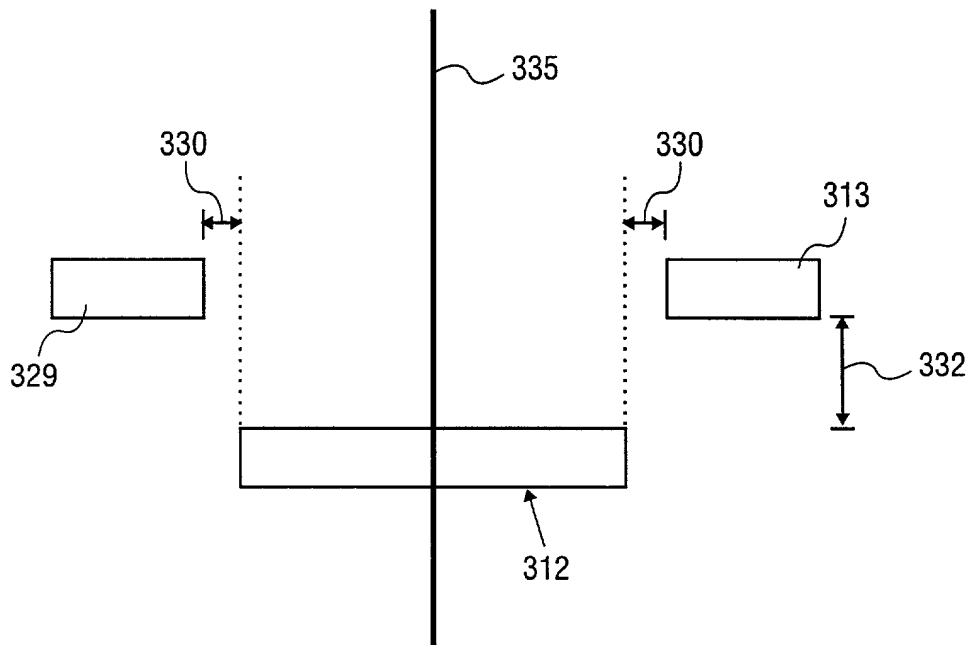
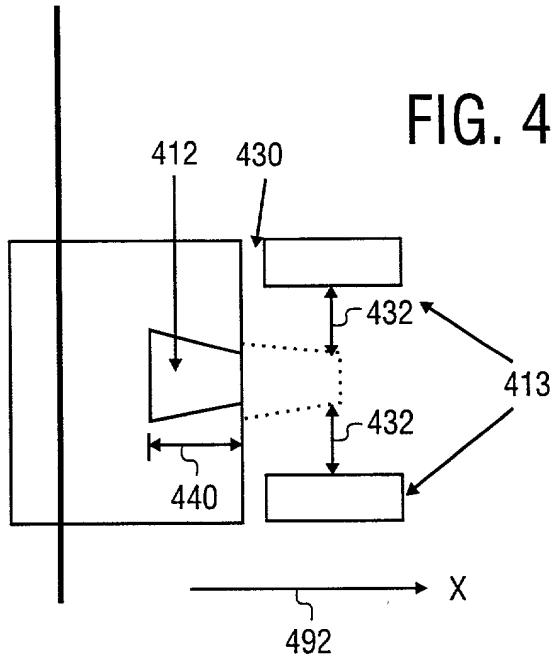


FIG. 3E

FIG. 4 is a schematic diagram of a device 400 in a cross-sectional view. The device 400 includes a substrate 410, a gate stack 412, a gate electrode 413, a channel layer 414, a source/drain region 415, and a contact layer 416. The gate stack 412 is formed on the substrate 410 and includes a gate oxide layer 412a and a gate electrode layer 412b. The gate electrode 413 is formed on the gate stack 412 and is connected to the gate oxide layer 412a. The channel layer 414 is formed on the gate electrode 413 and is connected to the gate electrode layer 412b. The source/drain region 415 is formed on the channel layer 414 and is connected to the channel layer 414. The contact layer 416 is formed on the source/drain region 415 and is connected to the source/drain region 415. The device 400 is shown in a cross-sectional view along a line X-X'.



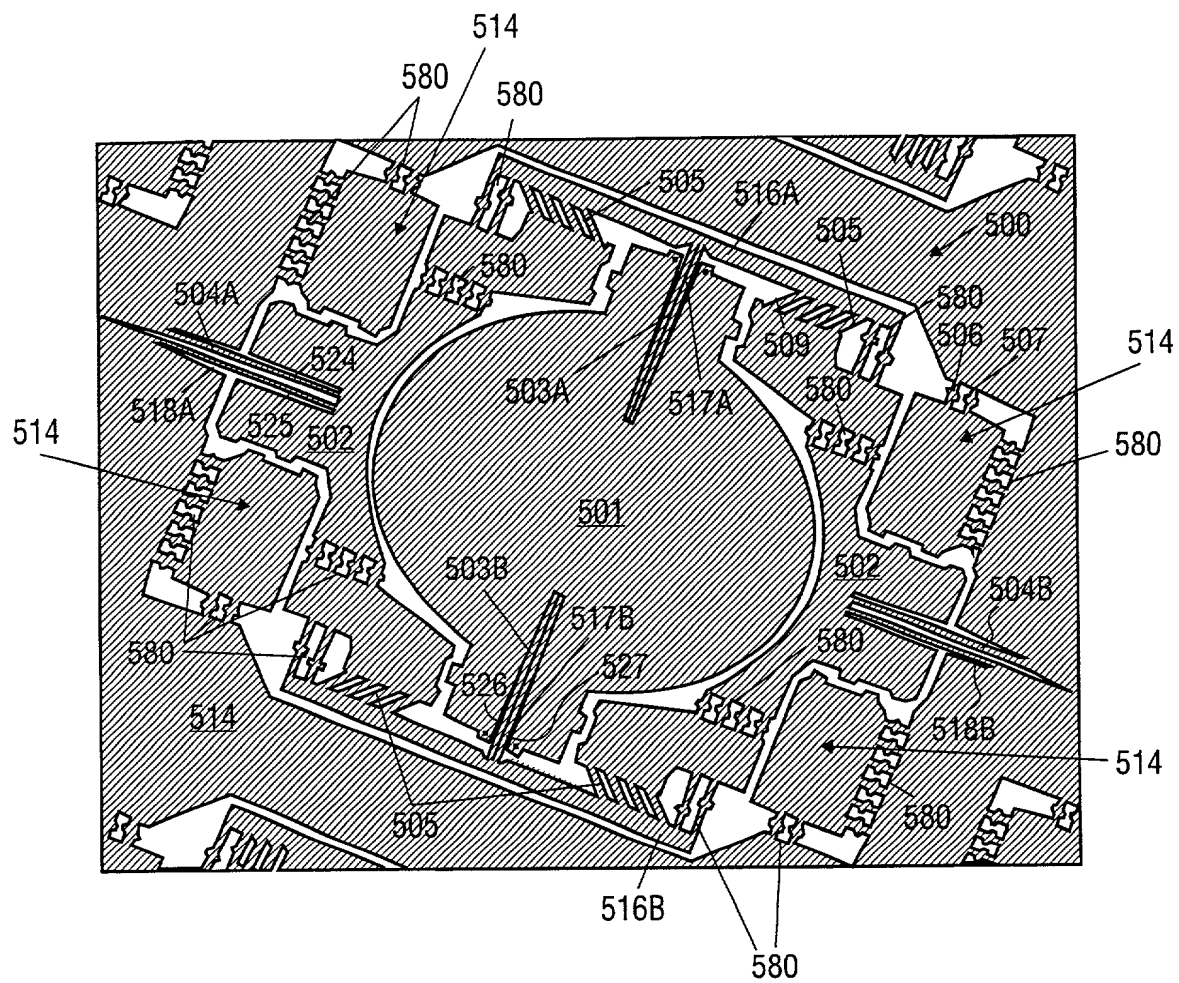


FIG. 5A

FIG. 5B is a cross-sectional view of the device 500 taken along line 500A of FIG. 5A, showing the device 500 in a first position. The device 500 includes a substrate 501, a gate stack 502, a channel layer 503, and a drain region 504. The gate stack 502 is formed on the substrate 501 and includes a gate dielectric layer 505 and a gate electrode layer 506. The channel layer 503 is formed on the gate stack 502 and includes a channel region 507 and a source region 508. The drain region 504 is formed on the channel layer 503 and includes a drain region 509 and a source region 510. The device 500 is shown in a first position, where the channel layer 503 is in contact with the gate stack 502 and the drain region 504 is in contact with the source region 510.

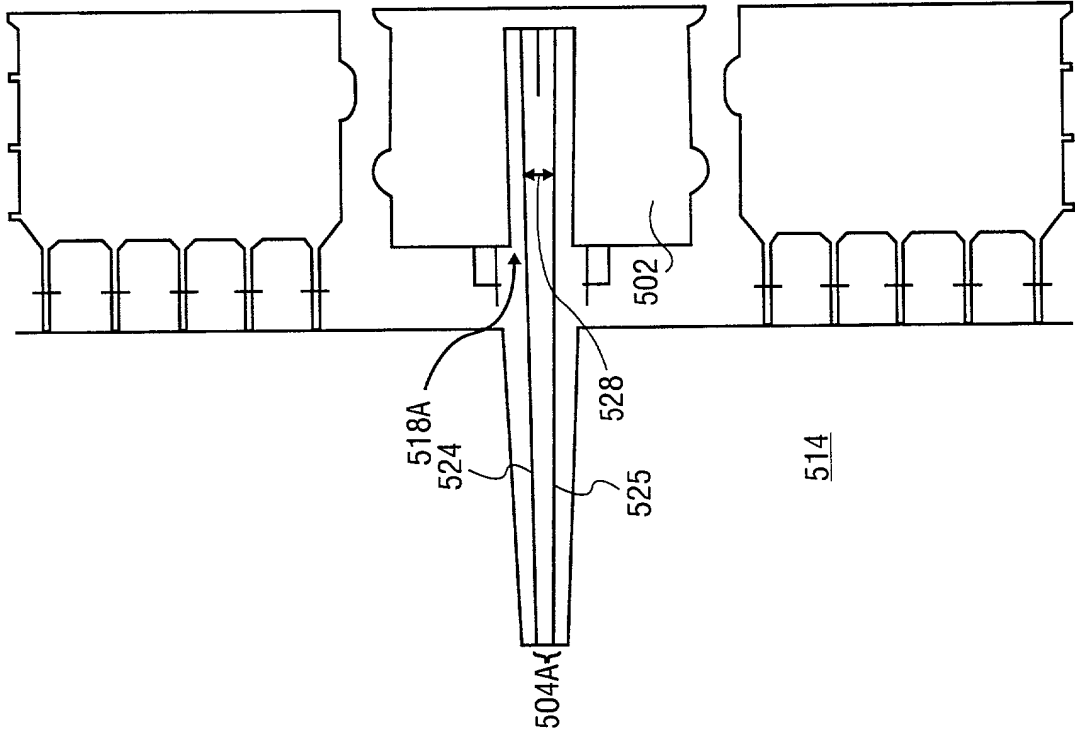


FIG. 5B

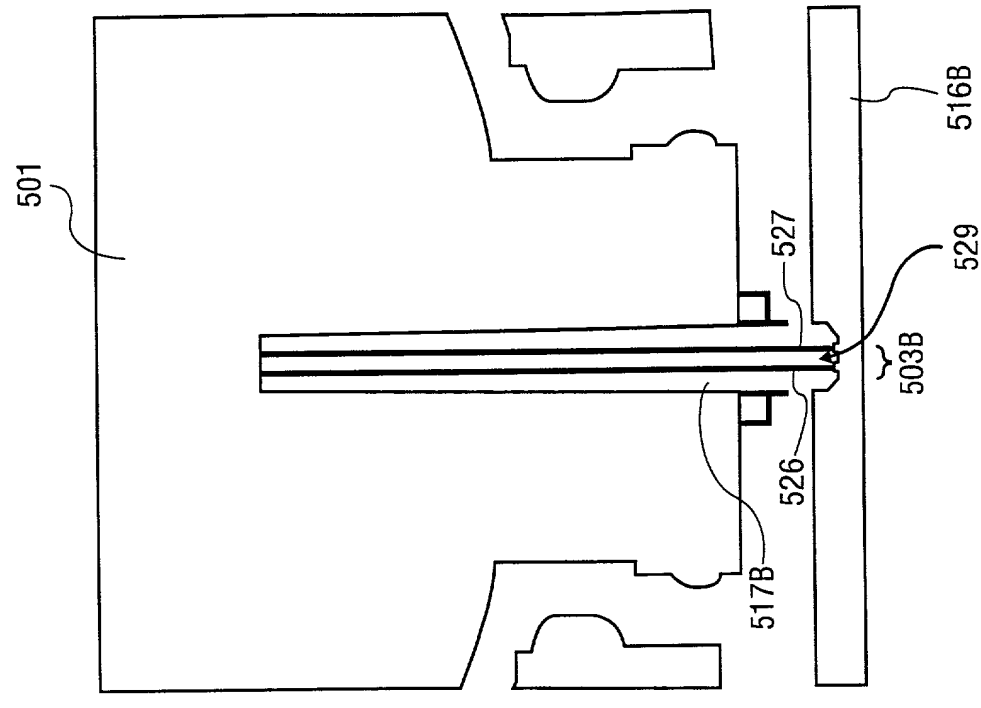


FIG. 5C

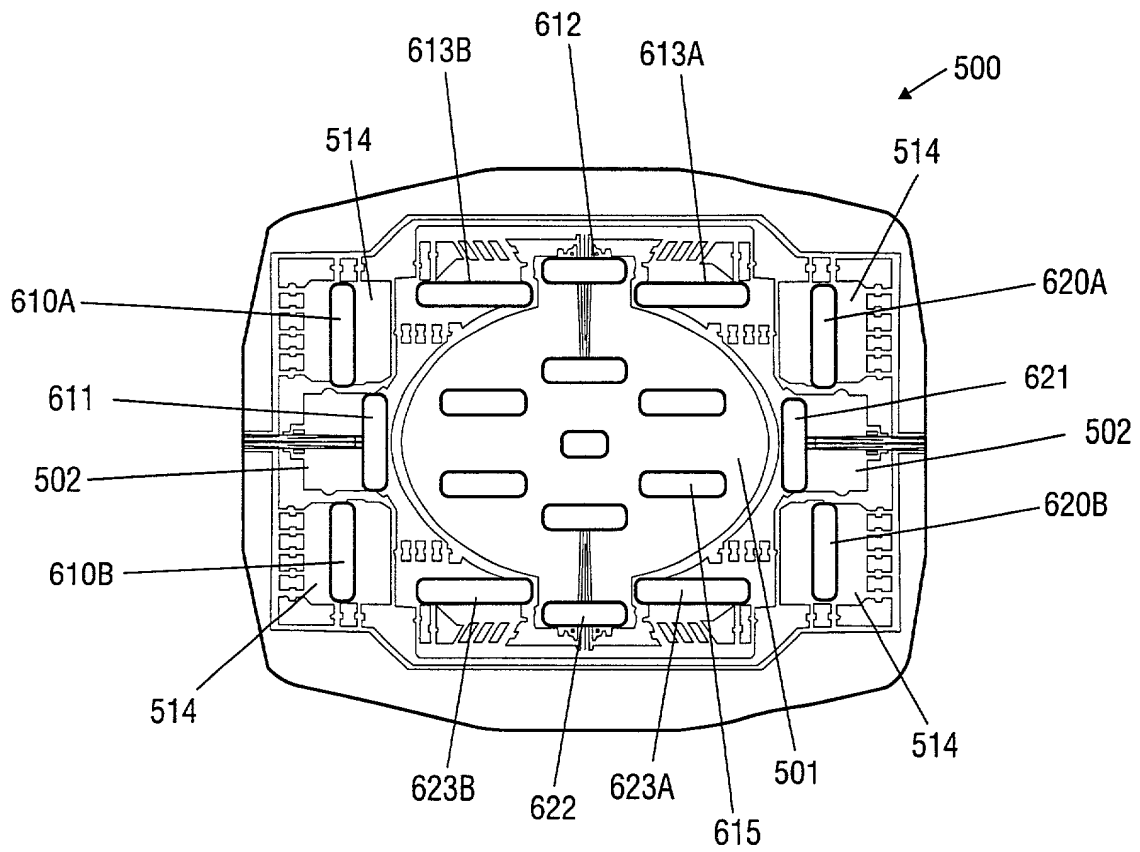


FIG. 6

FIG. 7A is a top view of a semiconductor device 700. The device 700 includes a substrate 701, a gate stack 702, a source/drain region 703, a gate electrode 704, a gate spacer 705, a gate contact 706, a gate pad 707, a gate line 708, a gate bus 709, a gate pad 710, a gate contact 711, a gate spacer 712, a gate electrode 713, a source/drain region 714, a gate stack 715, and a substrate 716.

700

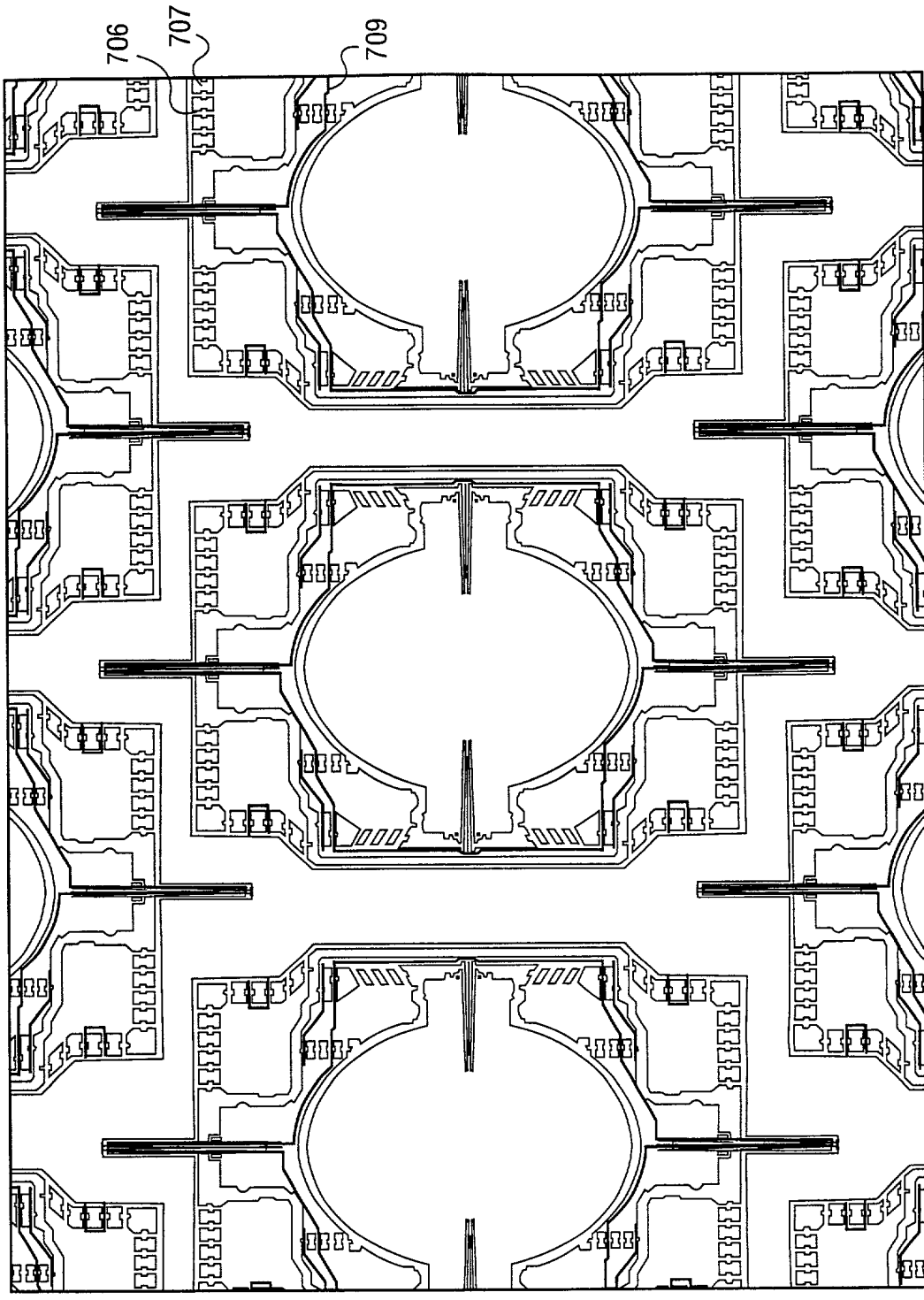


FIG. 7A

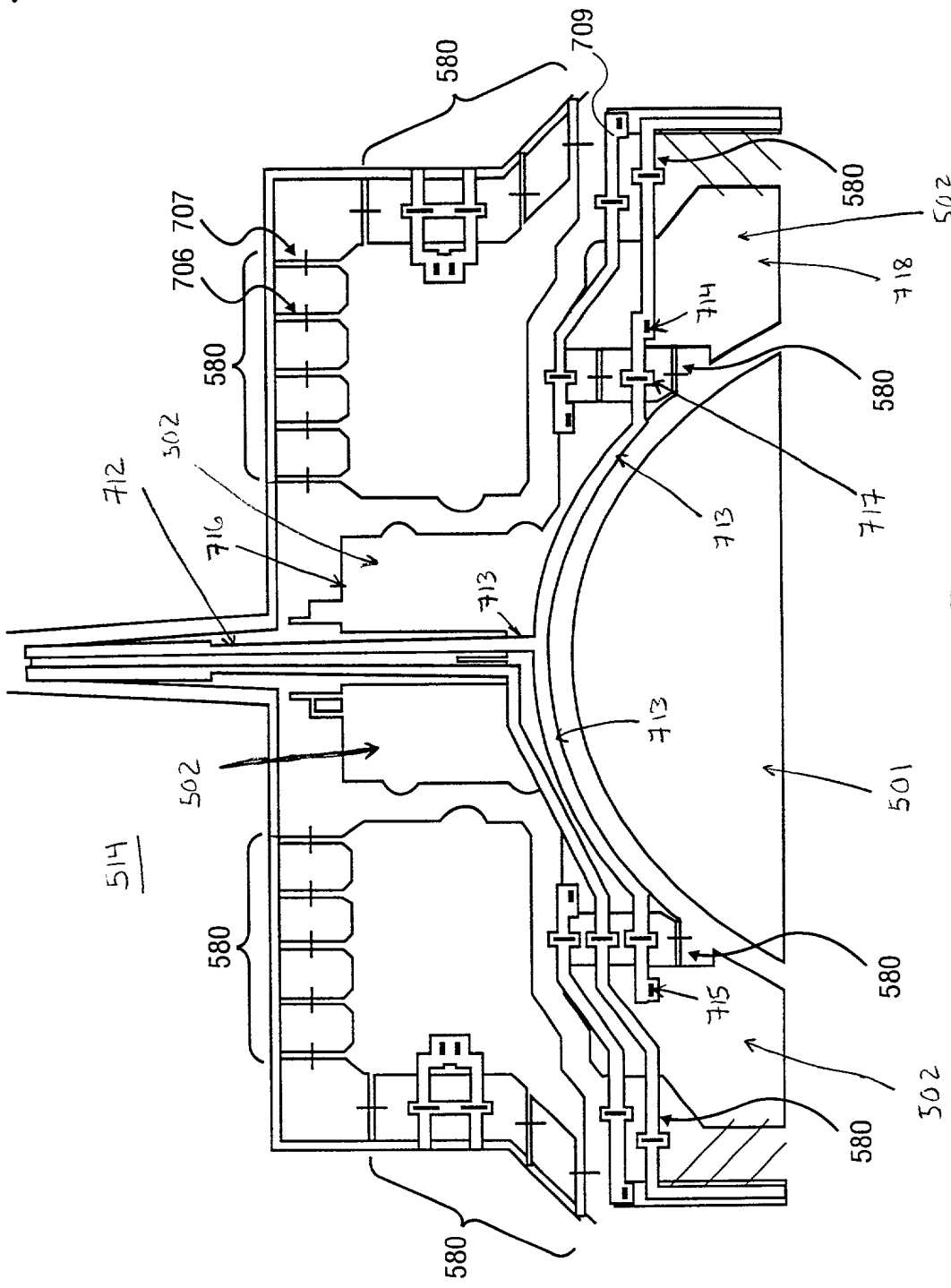


FIG. 7B

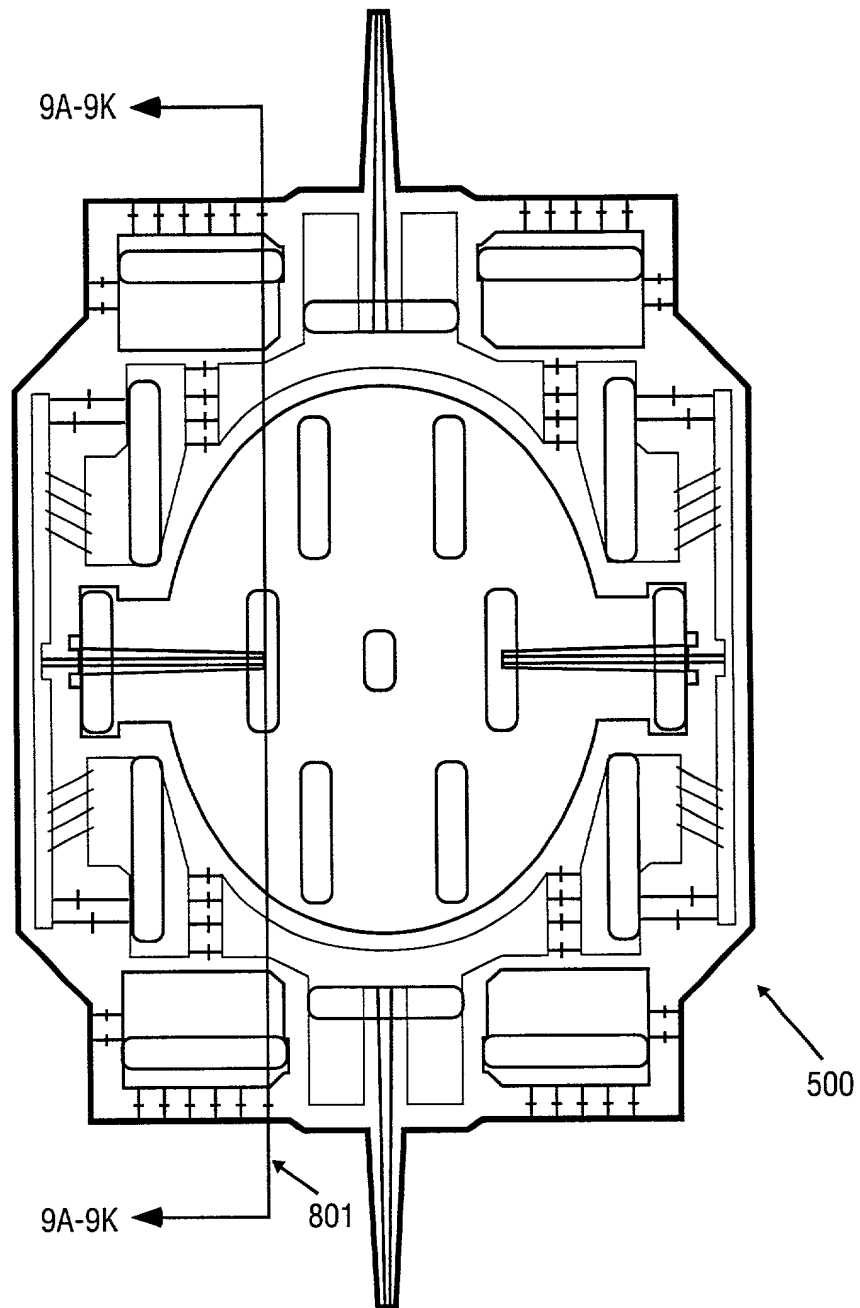


FIG. 8

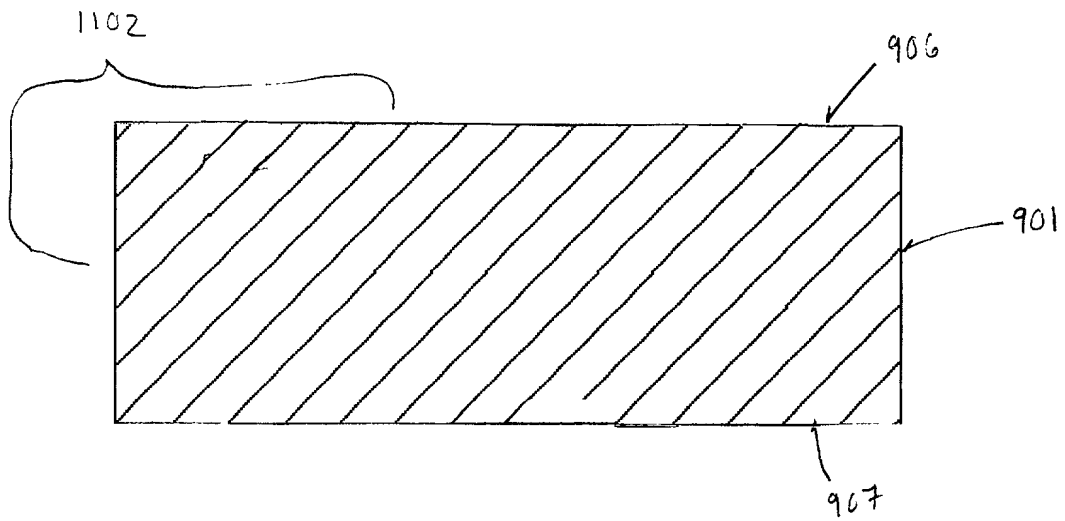


FIG. 9 A

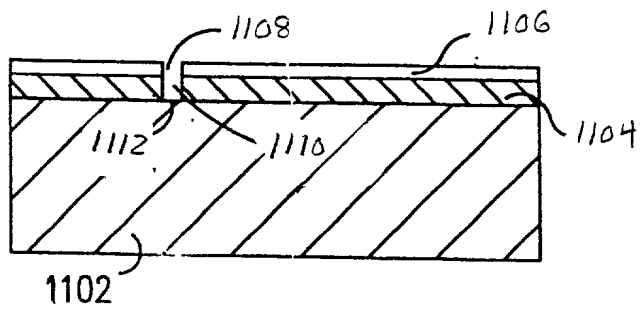


FIG. 9B

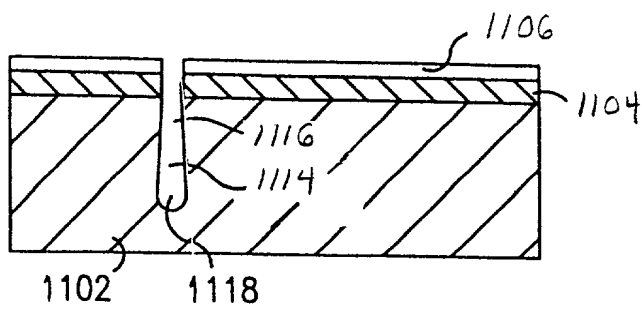


FIG. 9C

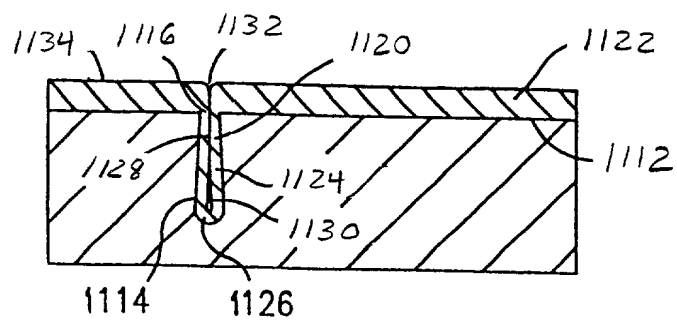


FIG. 9D

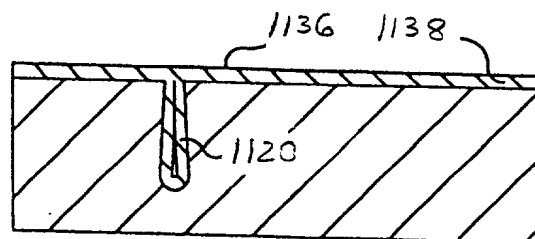
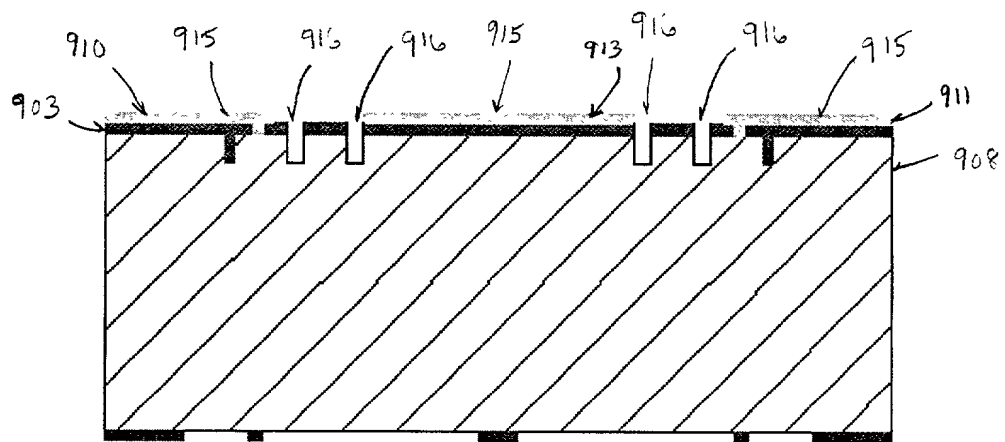
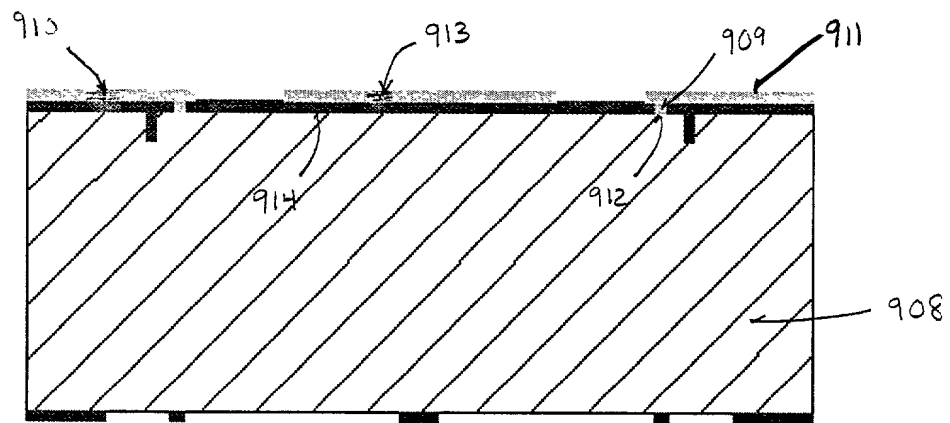
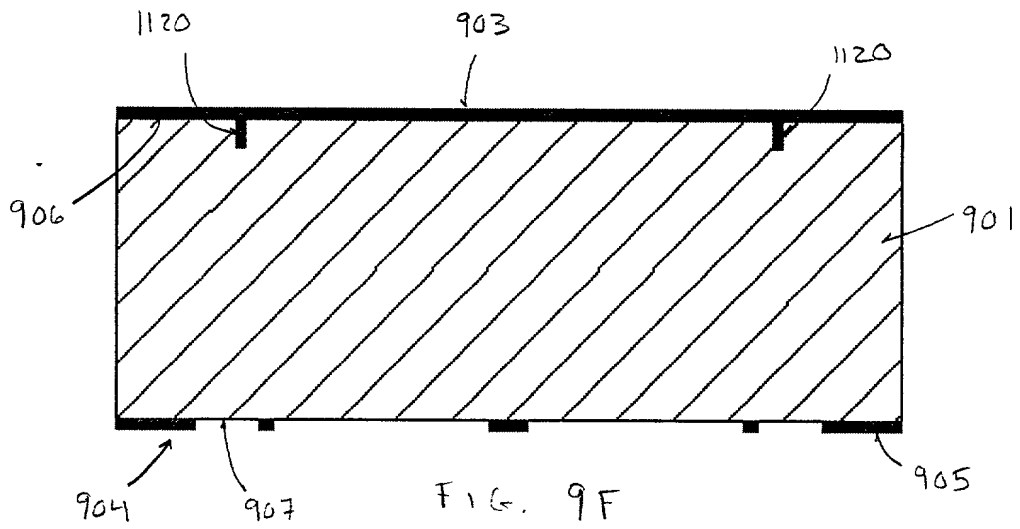
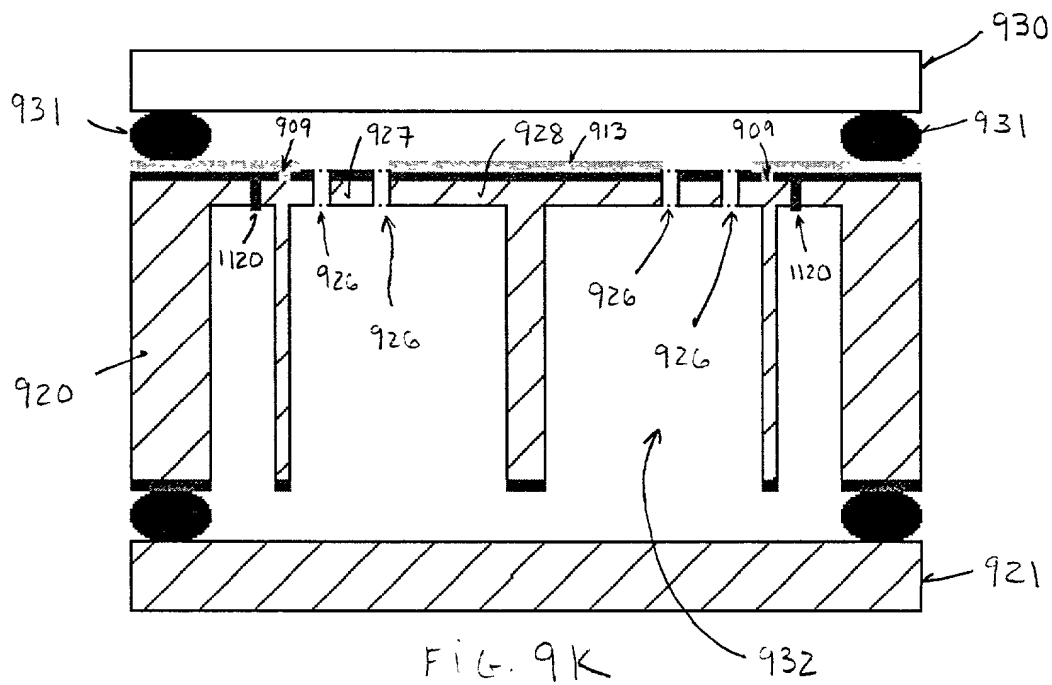
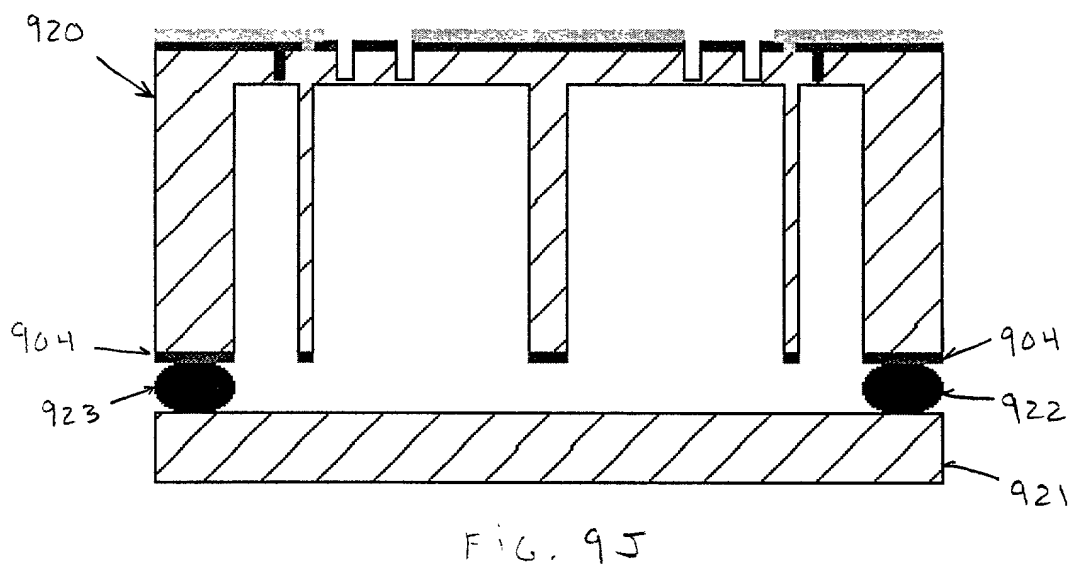
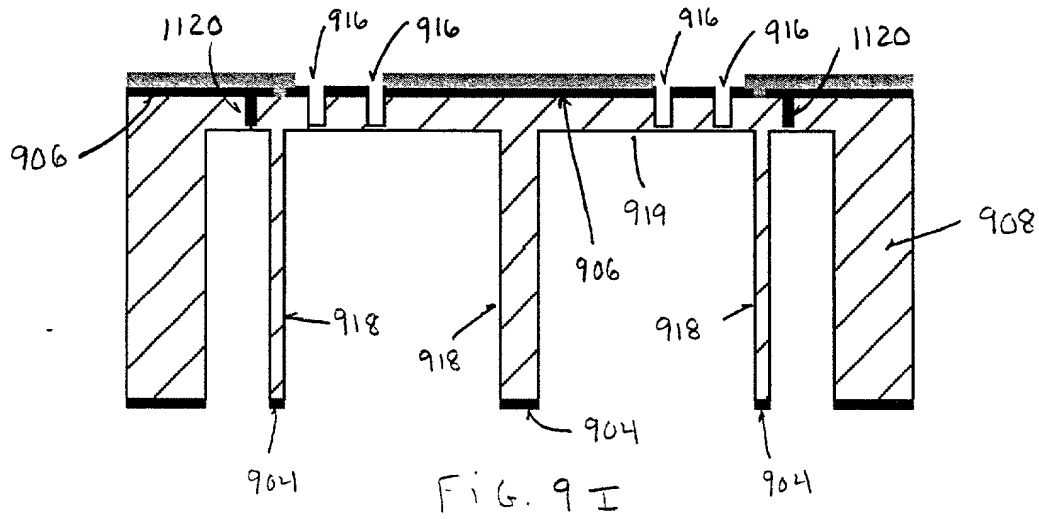
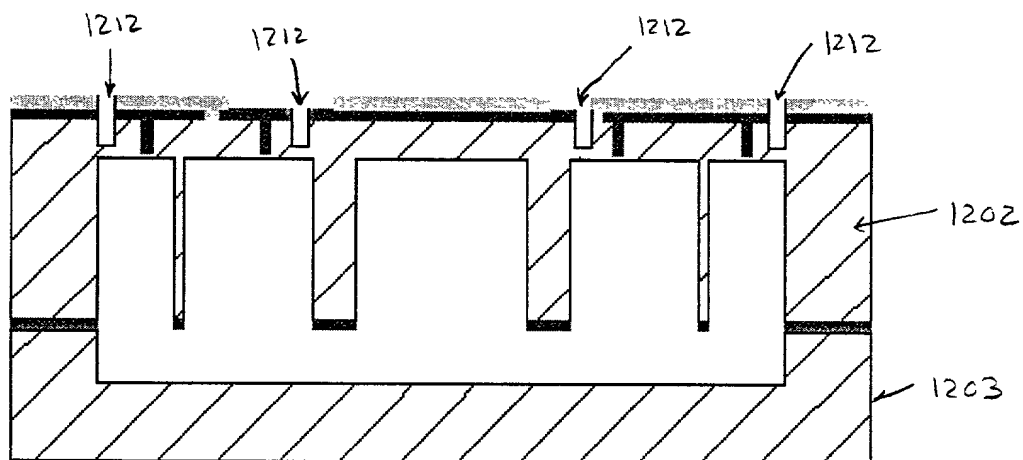
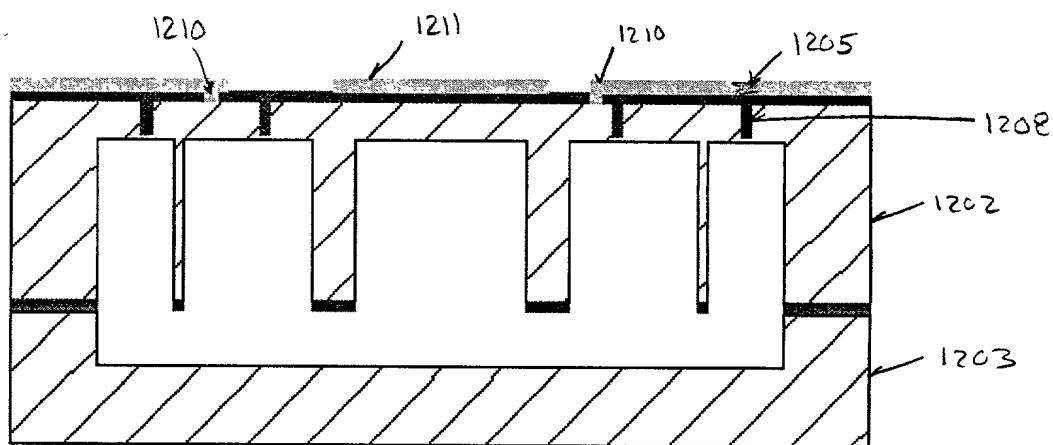
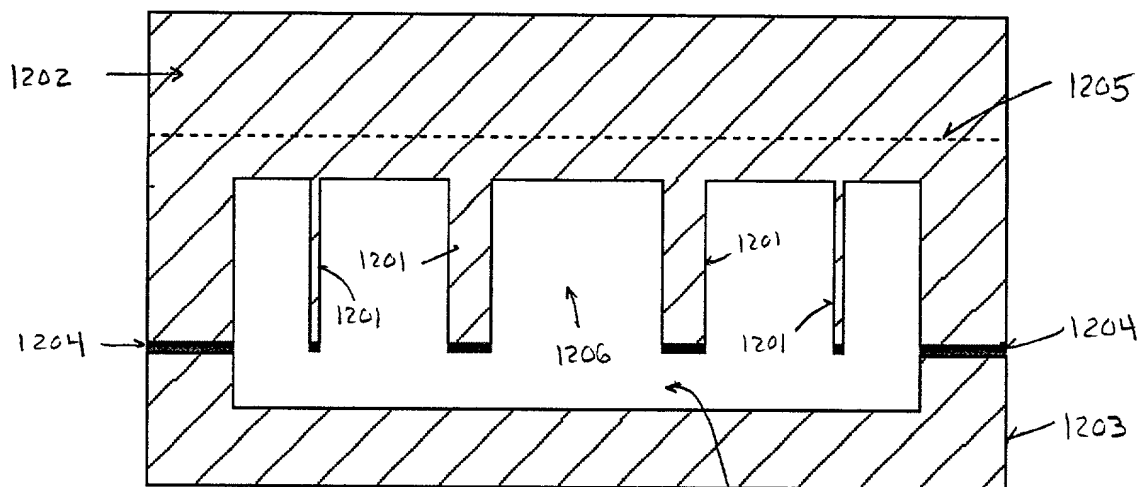


FIG. 9E







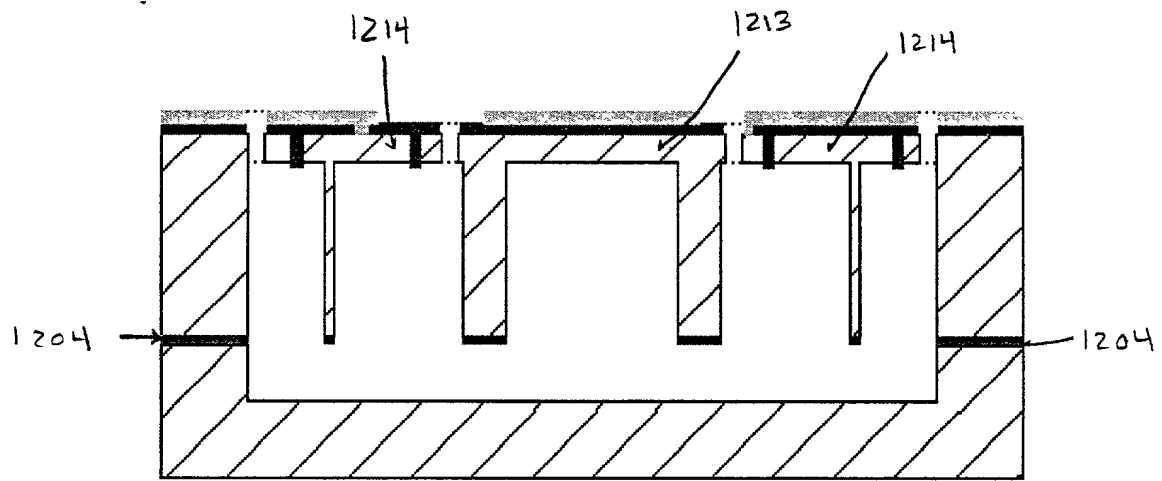


FIG. 10D

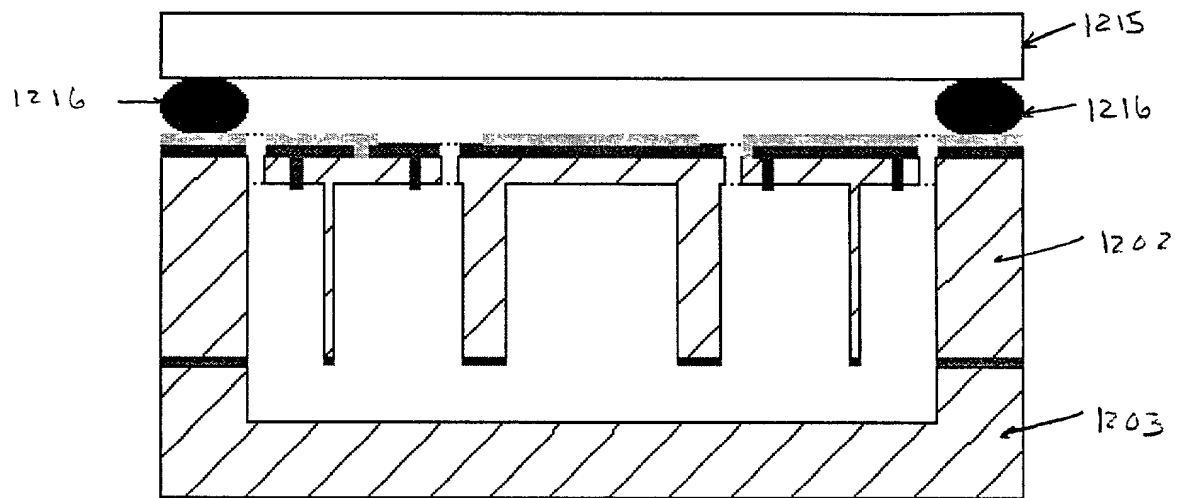


FIG. 10E

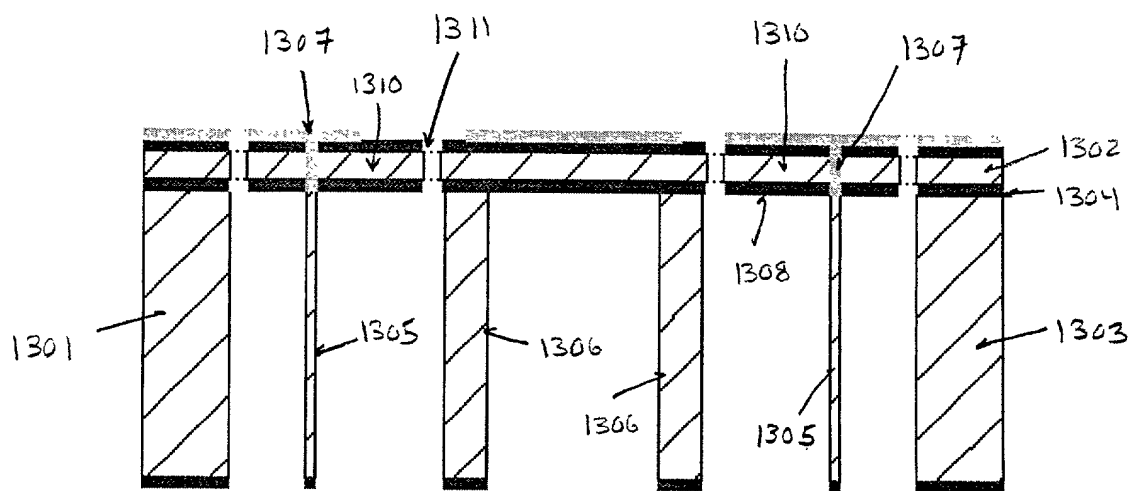
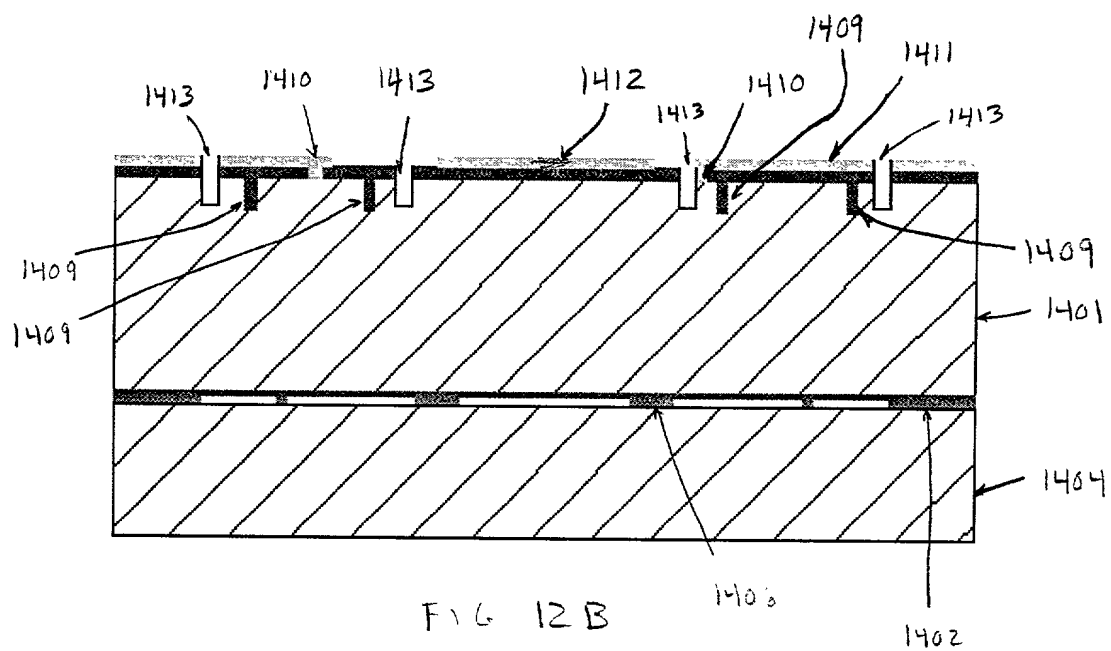
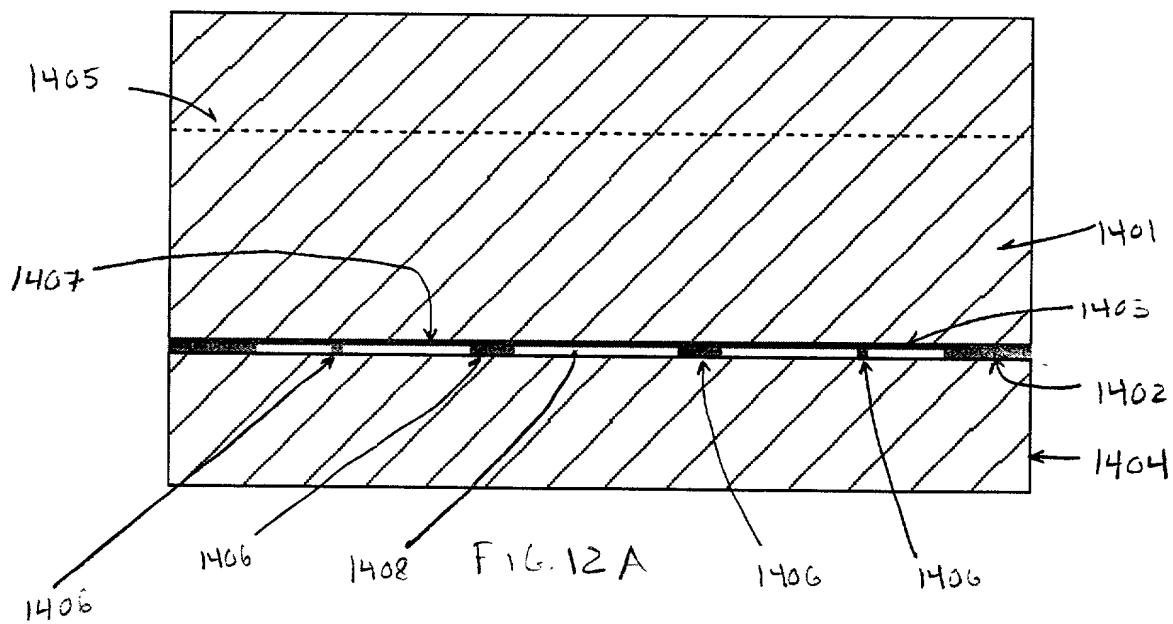


FIG. 11



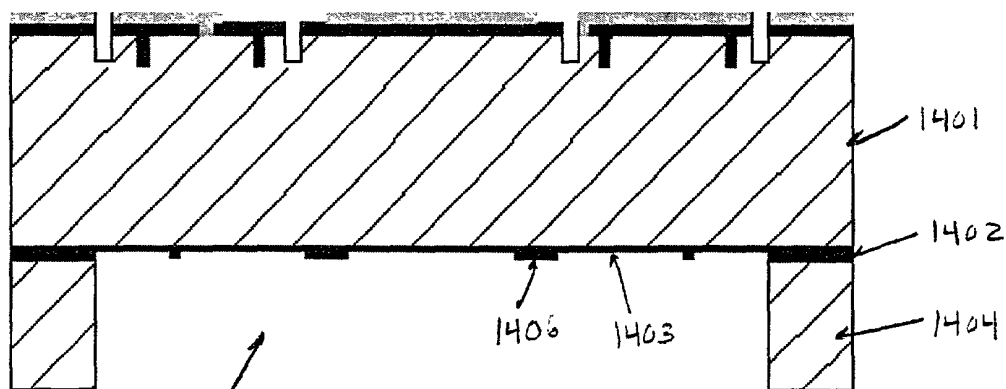


FIG. 12C

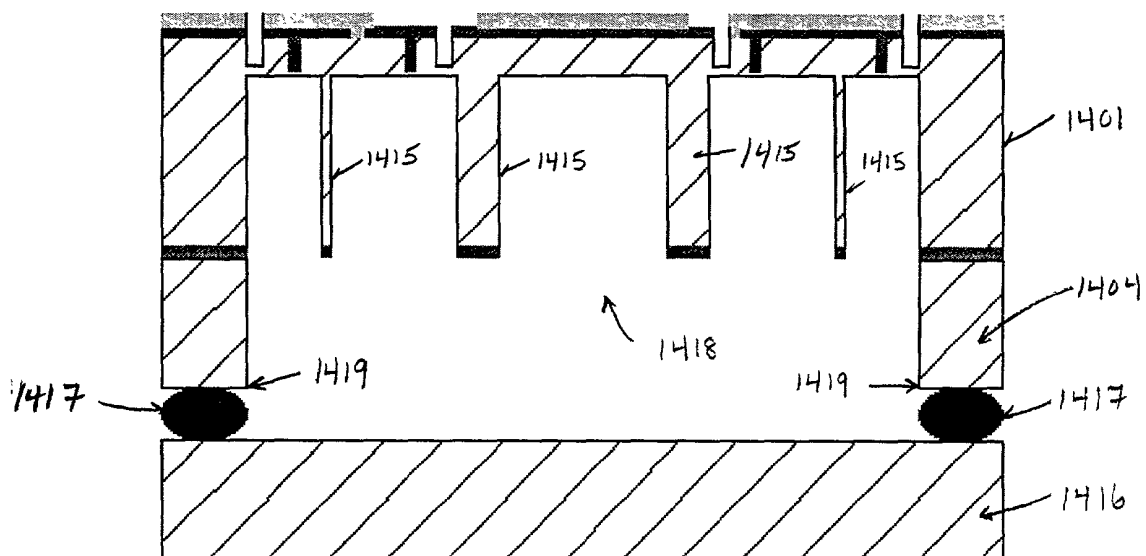


FIG. 12D

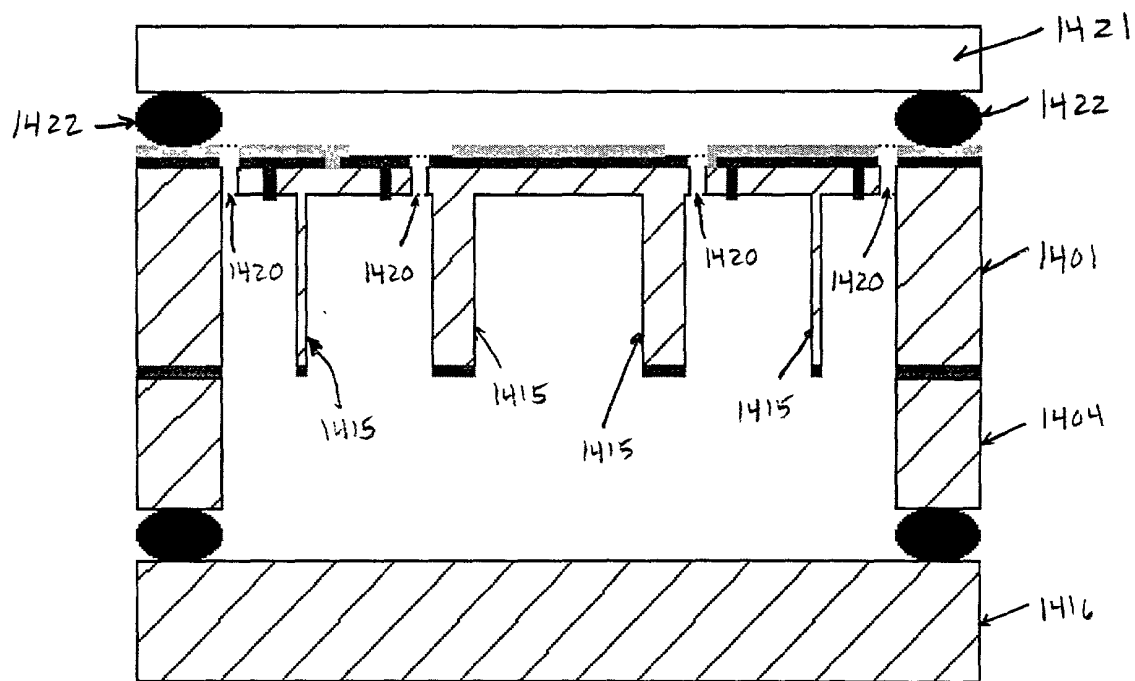


FIG 12E

FIG. 13A

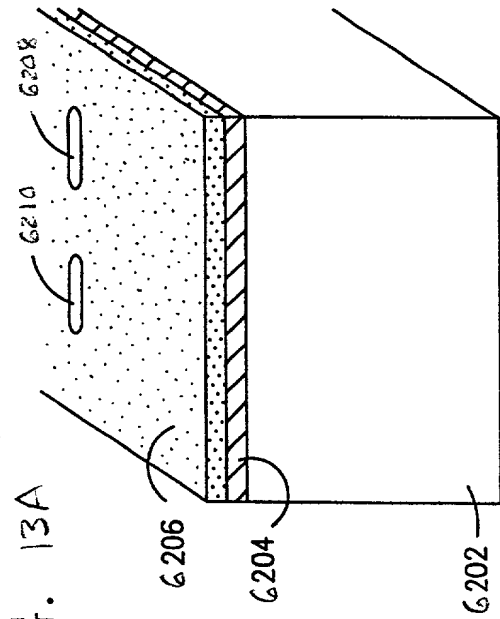


FIG. 13C

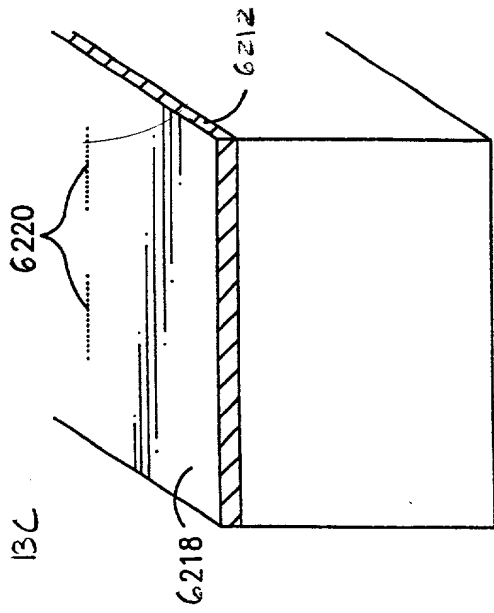


FIG. 13B

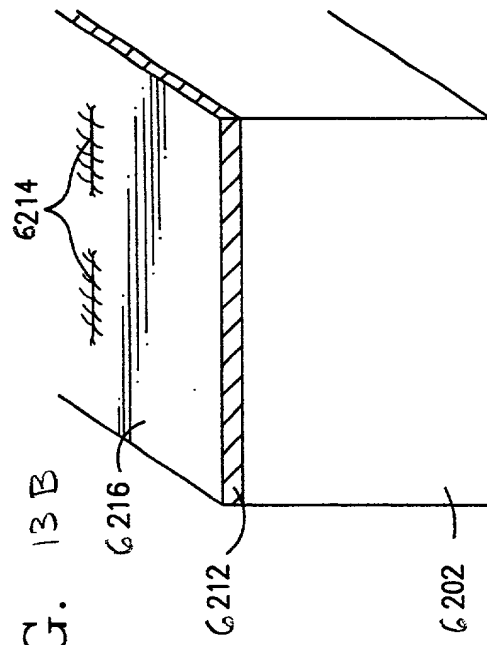


FIG. 13D

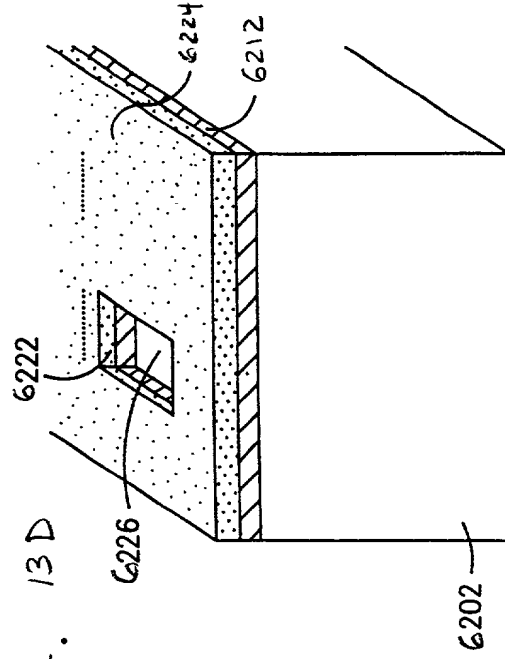


FIG. 13E

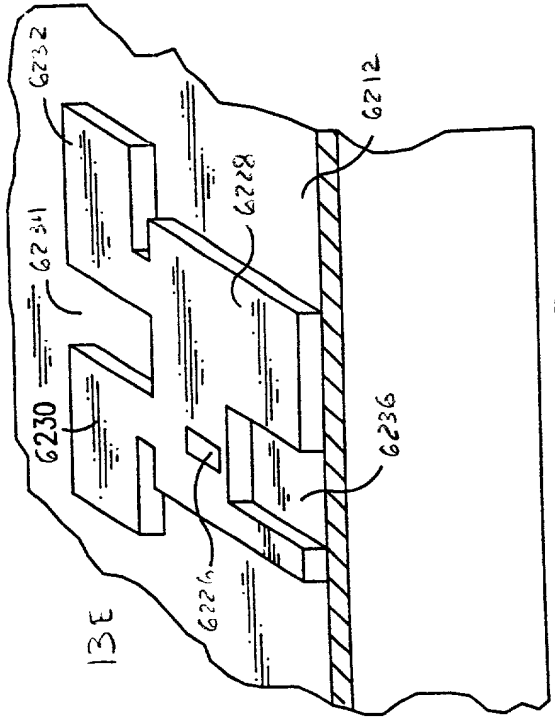


FIG. 13E

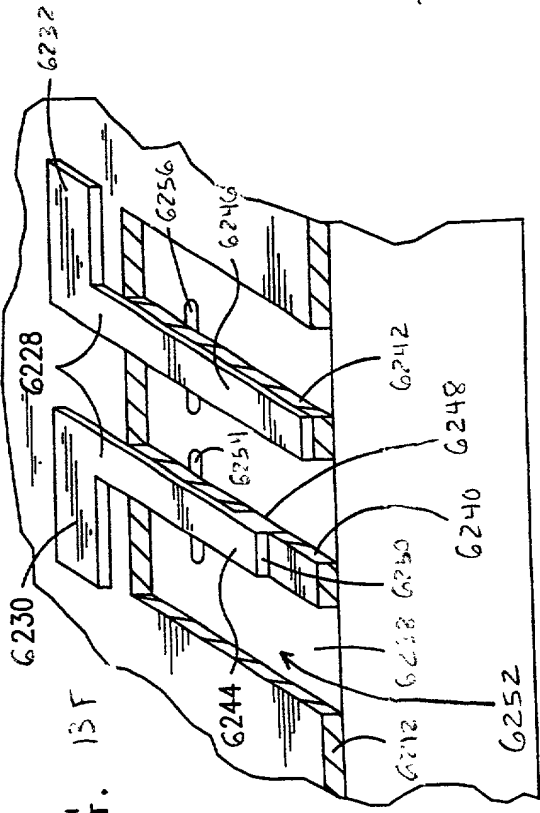


FIG. 13F

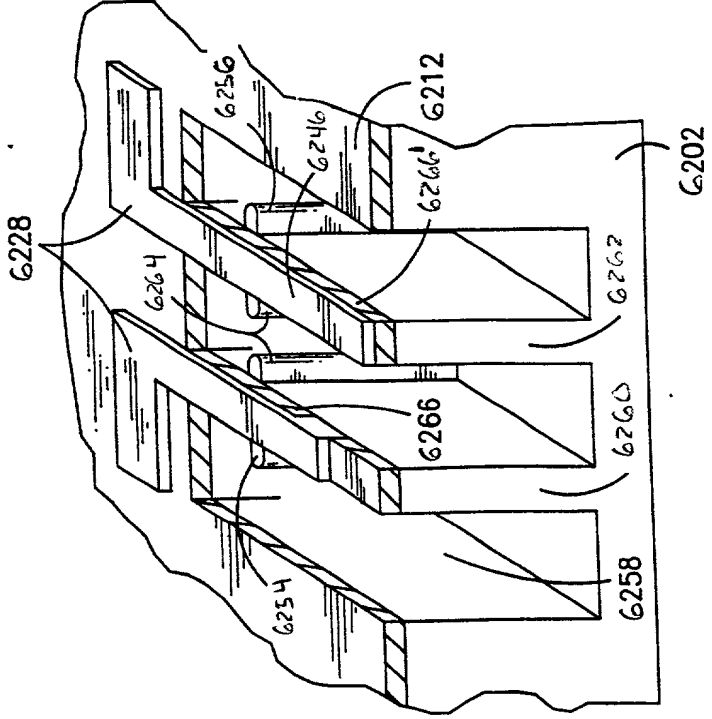


FIG. 13G

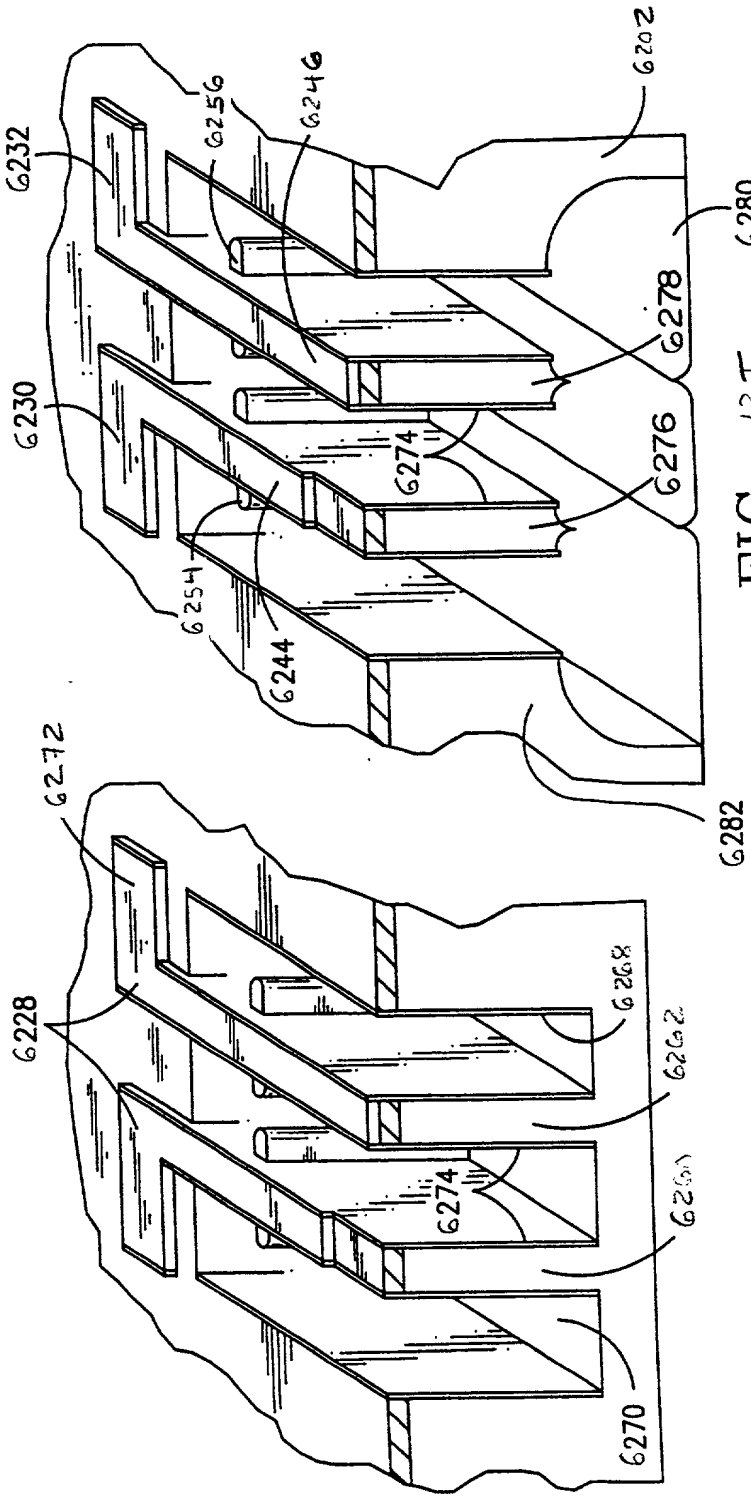


FIG. 13H

FIG. 13I